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EXAMINER
CRAIG, DWIN M

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 09/29/2003

11

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/475,717	NARDIN ET AL.	
	Examiner	Art Unit	
	Dwin M Craig	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *2-25-2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) *2,7,13,19,21,23,25 and 27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-6, 8-12, 14-18, 20, 22, 24, 26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *04 March 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 21, 23, 25 and 27 have been cancelled and withdrawn from consideration as per Applicant's request. Claims 1, 3, 4, 5, 6, 8, 9, 10, 11, 12, 14, 15, 16, 17, 18, 20, 22, 24 and 26 have been presented for reconsideration in light of Applicants amended claim language. Claims 1, 3, 4, 5, 6, 8, 9, 10, 11, 12, 14, 15, 16, 17, 18, 20, 22, 24 and 26 have been reconsidered and rejected.

Response to Arguments

2.

2.1 Regarding Applicant's submission of amended drawings;

The Examiner received formal drawings on 4 March 2003. The Examiner accepts the new drawings as formal and withdraws the previous objection.

2.2 Regarding Applicant's response to the 35 U.S.C. 103(a) rejections of Claims 1, 3-6, 8 and 9:

The Applicant has argued that:

> Claims 1, 3-6, 8 and 9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,363,515 to Rajgopal et al. ("Rajgopal") in view of U.S. Patent No. 5,828,579 to Beausang.
>
> "To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. All words in a claim must be considered in judging the patentability of that claim against the prior art." M.P.E.P. § 2143.03.
>
> Amended independent claim 1 now recites, in pertinent part, "reporting results of the simulating indicating whether any of the domino logic circuits is likely to generate an erroneous output ...." Applicants respectfully submit that the combination of Rajgopal and Beausang fails to disclose the aforementioned elements of claim 1. In fact, independent claim 1 now recites the elements of previously objected to claim 19. The Examiner indicated that claim 19 "would be allowable if rewritten in independent form ...." Office Action mailed March 31, 2003, page 12, section 6. Accordingly, Applicants request that the instant § 103 rejection of claim 1 be withdrawn.

> Amended independent claim 4 now recites, in pertinent parts, "determining whether any of the domino logic circuits is likely to generate an erroneous output." Applicants respectfully submit that the combination of Rajgopal and Beausang fails to disclose the aforementioned elements of claim 4. Claim 4 now includes elements of previously objected to claim 21. Accordingly, Applicants request that the instant § 103 rejection of claim 4 be withdrawn.

The Examiner asserts that Applicant's arguments are persuasive in that the both the *Rajgopal* reference and the *Beausang* reference disclose *"reporting results of the simulation indicating whether any of the domino logic circuits are likely to generate an erroneous output."* The Examiner withdraws the earlier 35 U.S.C. 103(a) rejections of Claims 1, 3-6, 8 and 9.

2.3 Regarding Applicant's response to the 35 U.S.C. 103(a) rejections of Claims 10-12 and 14-17:

The Applicant has argued that:

> Claims 10-12 and 14-17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Rajgopal in view of Beausang and if further view of U.S. Patent No.: 5,999,714 to Conn et al. ("Conn").
>
> Amended independent claim 10 now recites, in pertinent parts, "determining whether any of the domino logic circuits is likely to generate an erroneous output." Applicants respectfully submit that the combination of Rajgopal, Beausang, and Conn fails to disclose the aforementioned element of claims 10. Claim 10 now includes similar elements of previously objected to claim 23. Accordingly, Applicants request that the instant § 103 rejection of claim 10 be withdrawn.
>
> Amended independent claim 15 now recites, in pertinent part, "reporting results of the simulating indicating whether any of the domino logic circuits is likely to generate an erroneous output." For the reasons discussed above, Applicants request that the § 103 rejection of claim 15 be withdrawn.
>
> Amended independent claim 17 now recites, in pertinent part, "means for reporting results of the means for simulating, the results indicating whether any of the domino logic circuits is likely to generate an erroneous output." For the reasons discussed above, Applicants request that the § 103 rejection of claim 17 be withdrawn.

The Examiner asserts that Applicant's arguments are persuasive in that either the Rajgopal or the *Beausang* references expressly disclose, *"reporting results of the simulation indicating whether any of the domino logic circuits are likely to generate an erroneous output."*

The Examiner has found Applicant's arguments to be persuasive and withdraws the earlier 35 U.S.C. 103(a) rejections of claims 10-12 and 14-17.

2.4 Regarding Applicant's response to the 35 U.S.C. 103(a) rejections of dependent Claims 3, 5, 6, 8, 9, 11, 12, 14, 16, 18, 20, 22, 24, and 26:

The Applicant has argued that:

> Dependent claims 3, 5, 6, 8, 9, 11, 12, 14, 16, 18, 20, 22, 24, and 26 are nonobvious over the prior art of record for at least the same reasons as discussed above in connection with their respective independent claims, in addition to adding further limitations of their own. Accordingly, Applicants respectfully request that the instant § 103 rejections for claims 3, 5, 6, 8, 9, 11, 12, 14, 16, 18, 20, 22, 24, and 26 be withdrawn.

The Examiner asserts that Applicant's arguments are persuasive and withdraws the earlier 35 U.S.C. 103(a) rejections of Claims 3, 5, 6, 8, 9, 11, 12, 14, 16, 18, 20, 22, 24, and 26.

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are

such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 1, 3, 4, 5, 6, 8, 9, 18 and 20** are rejected under **35 U.S.C. 103(e)** as being unpatentable over **Rajgopal et al. U.S. Patent 6,363,515** in view of **Beausang U.S. Patent 5,828,579** and in further view of **"Validation and Test Generation for Oscillatory Noise in VLSI Interconnects" by Arani Sinha, Sandeep K. Gupta and Melvin A. Breuer** hereafter referred to as the *Sinha et al.* reference.

3.1 As regards independent **Claims 1 and 4** the *Rajgopal et al.* reference discloses simulating each domino circuit of a set of domino circuits **(Col. 3 Lines 65-67 and Col. 4 Lines 1-22),** and reporting the results **(Figure 1, Col. 7 Lines 26-39)** and discloses domino logic circuit having a set of inputs and an output and simulating each domino logic circuit after any circuits coupled to the set of inputs have been simulated, **(Col. 2 Lines 15-20 and Col. 3 Lines 58-65).** The *Rajgopal et al.* reference discloses parameter extraction **(Figure 1 Item 22).**

However, the *Rajgopal et al.* reference does not expressly disclose the limitation concerning analysis of domino circuits wherein each domino circuit is simulated in a specific order and the next domino circuit is analyzed using as an input the output of the last domino circuit that was analyzed and reporting results of the simulation indicating whether any of the domino logic circuits are likely to generate an erroneous output.

The *Beausang* reference discloses an analysis of circuits wherein the circuit is simulated in a specific order and next circuit analyzed is using the output of the last circuit that was analyzed according to an ordered list, **(Figures 6A, 6B, 7A, 7B, 8A, 8B, 9A, 9B, 10A, 10B, 11A,**

11B, 12A, 12B, 12C, 13A, 13B, 14A, 14B, Col. 3 Lines 1-12, Lines 58-67, Col. 4 Lines 1-15, Col. 21 Lines 10-34, Col. 39 Lines 46-67, Col. 40 Lines 1-7).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Rajgopal et al.* reference with the *Beausang* reference because *(motivation to combine)* the *Beausang* reference discloses a method wherein a user can modify a complex design, enter very specific design constraints and then verify a complex design in less time ***(Beausang Col. 2 Lines 21-67, Col. 3 Lines 1-12).***

The *Sinha et al.* reference discloses reporting results of the simulation indicating whether any of the domino logic circuits are likely to generate an erroneous output **(pp. 293 Procedure for Test Generation & pp.294 Test Generation Example).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have modified the *Rajgopal et al.* reference with the *Sinha et al.* reference because, the inductance of on-chip interconnects can lead to high levels of noise and there exists a need to test and validate a design to make certain that the noise magnitude stays below a level that will support proper chip functionality **(*Sinha et al. pp. 296 Conclusions*).**

3.2 As regards **Claim 3** the *Rajgopal et al.* reference discloses simulating each domino logic circuit including the simulated results of circuits coupled to the inputs of the domino logic circuit **(Col. 3 Lines 58-67, Col. 4 Lines 1-8).**

3.3 As regards **Claim 5** the *Rajgopal et al.* reference discloses parameter extraction **(Figure 1 Item 22).**

3.4 As regards **Claim 6** the *Rajgopal et al.* reference discloses a reporting of the results of the simulation, **(Figure 1, Col. 7 Lines 26-39).**

3.5 As regards **Claim 8** the *Rajgopal et al.* reference discloses extracting parameters **(Figure 1 Item 22),** an ordered list **(Figure 6 Item 72, Figure 5 and Figure 4)** the Examiner asserts that a NETLIST is an ordered list, and simulating non-domino circuits **(Figure 6 Item 81)** the Examiner asserts that the buffers being inserted are not, in and of themselves domino circuits.

3.6 As regards **Claim 9** the *Rajgopal et al.* reference discloses simulating non-domino circuits **(Figure 6 Item 81)** the Examiner asserts that the buffers being inserted are not, in and of themselves domino circuits, and reporting the results of simulating the non-domino circuits **(Figure 1, Col. 7 Lines 26-39).**

3.7 As regards dependent **Claims 18 and 20** the *Rajgopal et al.* reference does not expressly disclose determining *worst-case noise.*

The *Sinha et al.* reference discloses *worst-case noise* **(pp. 293 Procedure for Test Generation).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have modified the *Rajgopal et al.* reference with the *Sinha et al.* reference because, the inductance of on-chip interconnects can lead to high levels of noise and there exists a need to test and validate a design to make certain that the noise magnitude stays below a level that will support proper chip functionality ***(Sinha et al. pp. 296 Conclusions).***

4. **Claims 10, 11, 12, 14, 15, 16, 17, 22, 24 and 26** are rejected under **35 U.S.C. 103(e)** over **Rajgopal et al. U.S. Patent 6,363,515** in view of and in further view of **Beausang U.S. Patent 5,828,579** and in further view of **Conn et al. U.S. Patent 5,999,714** and in further view of

"Validation and Test Generation for Oscillatory Noise in VLSI Interconnects" by Arani Sinha, Sandeep K. Gupta and Melvin A. Breuer hereafter referred to as the *Sinha et al.* reference.

4.1 As regards independent **Claims 10, 15 and 17** the *Rajgopal et al.* reference discloses simulating each domino circuit of a set of domino circuits **(Col. 3 Lines 65-67 and Col. 4 Lines 1-22),** and reporting the results **(Figure 1, Col. 7 Lines 26-39)** and discloses domino logic circuit having a set of inputs and an output and simulating each domino logic circuit after any circuits coupled to the set of inputs have been simulated, **(Col. 2 Lines 15-20 and Col. 3 Lines 58-65).** The *Rajgopal et al.* reference discloses parameter extraction **(Figure 1 Item 22).**

However, the *Rajgopal et al.* reference does not expressly disclose the limitation concerning analysis of domino circuits wherein each domino circuit is simulated in a specific order and the next domino circuit is analyzed using as an input the output of the last domino circuit that was analyzed and reporting results of the simulation indicating whether any of the domino logic circuits are likely to generate an erroneous output.

The *Beausang* reference discloses an analysis of circuits wherein the circuit is simulated in a specific order and next circuit analyzed is using the output of the last circuit that was analyzed according to an ordered list, **(Figures 6A, 6B, 7A, 7B, 8A, 8B, 9A, 9B, 10A, 10B, 11A, 11B, 12A, 12B, 12C, 13A, 13B, 14A, 14B, Col. 3 Lines 1-12, Lines 58-67, Col. 4 Lines 1-15, Col. 21 Lines 10-34, Col. 39 Lines 46-67, Col. 40 Lines 1-7).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Rajgopal et al.* reference with the *Beausang* reference because *(motivation*

to combine) the *Beausang* reference discloses a method wherein a user can modify a complex design, enter very specific design constraints and then verify a complex design in less time ***(Beausang Col. 2 Lines 21-67, Col. 3 Lines 1-12).***

The *Sinha et al.* reference discloses reporting results of the simulation indicating whether any of the domino logic circuits are likely to generate an erroneous output **(pp. 293 Procedure for Test Generation & pp.294 Test Generation Example).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have modified the *Rajgopal et al.* reference with the *Sinha et al.* reference because, the inductance of on-chip interconnects can lead to high levels of noise and there exists a need to test and validate a design to make certain that the noise magnitude stays below a level that will support proper chip functionality ***(Sinha et al. pp. 296 Conclusions).***

4.2 As regards **Claim 10** the *Rajgopal et al.* reference does not expressly disclose a machine-readable medium.

The *Conn et al.* reference discloses a machine-readable medium **(Col. 2 Lines 22-42).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Rajgopal et al.* reference with the *Conn et al.* reference because *(motivation to combine)* the *Conn et al.* reference discloses a method of taking into consideration noise and performing circuit optimization that results in greater design efficiency ***(Conn et al. Col. 4 Lines 29-47).***

4.3 As regards **Claim 15** the *Rajgopal et al.* reference does not expressly disclose a processor, a memory controller coupled to the processor, and a memory coupled to the memory controller.

The *Conn et al.* reference discloses a processor, a memory controller coupled to the processor, and a memory coupled to the memory controller **(Col. 2 Lines 22-42).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Rajgopal et al.* reference with the *Conn et al.* reference because *(motivation to combine)* the *Conn et al.* reference discloses a method of taking into consideration noise and performing circuit optimization that results in greater design efficiency ***(Conn et al. Col. 4 Lines 29-47).***

4.4 As regards **Claim 17** the *Rajgopal et al.* reference does not expressly disclose an apparatus.

The *Conn et al.* reference discloses an apparatus **(Col. 2 Lines 22-42).**
It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Rajgopal et al.* reference with the *Conn et al.* reference because *(motivation to combine)* the *Conn et al.* reference discloses a method of taking into consideration noise and performing circuit optimization that results in greater design efficiency ***(Conn et al. Col. 4 Lines 29-47).***

4.5 As regards **Claims 11 and 16** the *Rajgopal et al.* reference discloses parameter extraction **(Figure 1 Item 22).**

4.6 As regards to **Claim 12** the *Rajgopal et al.* reference discloses reporting results **(Figure 1, Col. 7 Lines 26-39).**

4.7 As regards **Claim 14** the *Rajgopal et al.* reference discloses an ordered list **(Figure 6 Item 72, Figure 5 "Block Netlist for Adder")** the Examiner asserts that a NETLIST is an ordered list. The *Rajgopal et al.* reference discloses extracting parameters **(Figure 1 Item**

22), and simulating non-domino circuits **(Figure 6 Item 81)** the Examiner asserts that the buffers being inserted are not, in and of themselves domino circuits.

4.8 As regards dependent **Claims 22, 24 and 26** the *Rajgopal et al.* reference does not expressly disclose determining worst-case noise.

The *Sinha et al.* reference discloses *worst-case noise* **(pp. 293 Procedure for Test Generation).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have modified the *Rajgopal et al.* reference with the *Sinha et al.* reference because, the inductance of on-chip interconnects can lead to high levels of noise and there exists a need to test and validate a design to make certain that the noise magnitude stays below a level that will support proper chip functionality ***(Sinha et al. pp. 296 Conclusions).***

Conclusion

5. It is noted by the Examiner that IEEE published the *Sinha et al.* reference in November 1999.

5.1 The Applicant has changed the scope of the original claims and, in light of an updated search; the Examiner has applied new art rejections to Applicant's amended claims.

5.2 In view of the new art rejections this action is made **NON-FINAL.**

5.3 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwin M Craig whose telephone number is 703 305-7150. The examiner can normally be reached on 9:00 - 5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703 305-9704. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 305-3900.

DMC
September 9, 2003